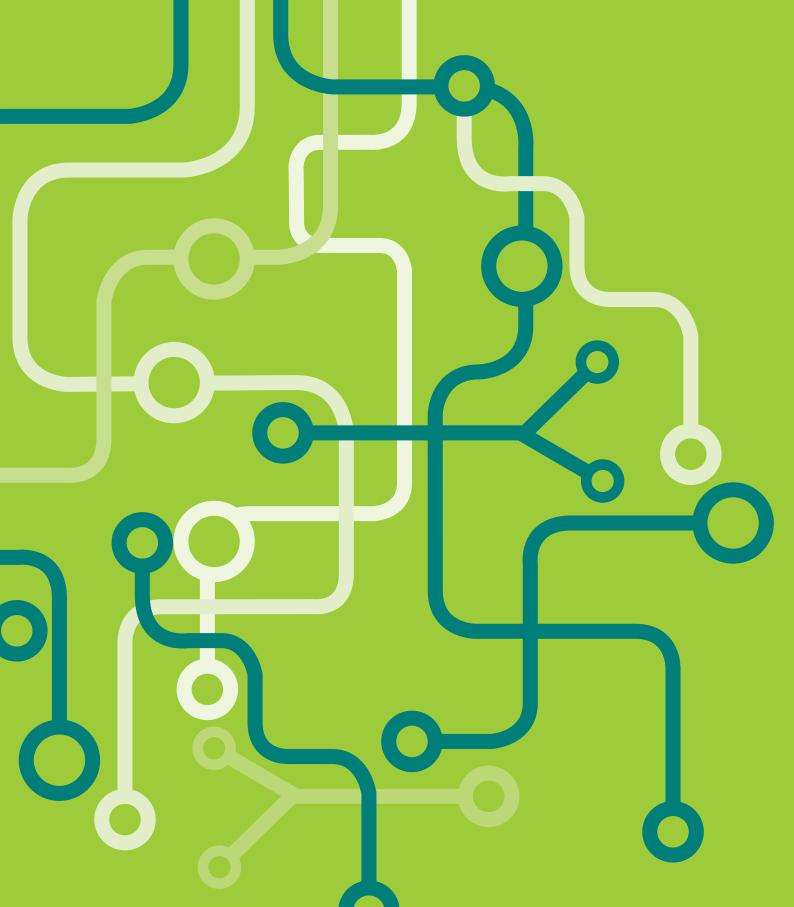


14-15 SEPTEMBER 2016
AUSTRALIAN
TECHNOLOGY PARK,
SYDNEY, AUSTRALIA



CONFERENCE PRESENTATIONS:

CONFERENCE PRESENTERS:

- > DEFECT ANALYSIS AND PROCESS TROUBLESHOOTING
- > CHARACTERISING AND MINIMISING VOIDS IN QFN DEVICE ASSEMBLY
- > ROOT CAUSE ANALYSIS FOR RELIABILITY ISSUES IN ELECTRONICS PACKAGING
- > DFX DESIGN FOR EXCELLENCE: DFM, DFA, DFT AND MORE
- > FLEX PCB DESIGN AND ASSEMBLY
- > HIGH PERFORMANCE DIGITAL CONTROL
- > INTERNET OF THINGS
- > ELECTRONIC DESIGN THROUGH COLLABORATION
- > GETTING YOUR PRODUCT TO MARKET FASTER WITH 3D PRINTING
- > SOLDERING TIPS FOR INCREASED YIELD AND RELIABILITY
- > IPC-A-610 ACCEPTABILITY OF ELECTRONIC ASSEMBLIES CERTIFICATION
- > ESD CONTROL WORKSHOP AND CERTIFICATION

DR S M RAMKUMAR
MR DALE LEE
DR HAMISH LAIRD
MR MARK STEINER
MR SIMON BLYTH
MR JOHN WHINNEN
MR MARK DOBSON
MR MIKE ROSS



ELECTRONEX EXHIBITION WILL BE OPEN ON WEDNESDAY 14TH SEPTEMBER - 10AM TO 6PM THURSDAY 15TH SEPTEMBER - 10AM TO 5PM DON'T MISS THE INDUSTRY'S KEY EXHIBITION!



















CONFERENCE PROGRAM

Tuesday September 13 IPC-A-610 Acceptability of Electronic Assemblies Day 1 of a 3 day course with Master IPC Trainer Mike Ross Pesign for Excellence: DFM, DFR, DFA and More with Dale Lee SMT and Through Hole Defect Analysis and Process Troubleshooting with Dr S Manian Ramkumar High Performance Digital Control with Dr Hamish Laird IPC-A-610 Acceptability of Electronic Assemblies Day 2 of a 3 day course Lunchtime presentation Getting your product to market faster with 3D Printing - John Whinnen Electronic Design through Collaboration - Mark Steiner CONFERENCE RECEPTION 6.15 PM REC Thursday September 15 Flex PCB Design and Assembly with Dale Lee Root Cause Analysis for Reliability Issues in Electronics Packaging with Dr S Maniam Ramkumar Lunchtime Presentation - Internet of Things - Simon Blyth Where'd the Heat Go? – Impacts of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon SOL	DATE	PROGRAM	TIMES	CODE	SEE PAGE
September 14 with Dale Lee SMT and Through Hole Defect Analysis and Process Troubleshooting with Dr S Manian Ramkumar High Performance Digital Control with Dr Hamish Laird 8.30 am to 4.30 pm DIG IPC-A-610 Acceptability of Electronic Assemblies Day 2 of a 3 day course Lunchtime presentation Getting your product to market faster with 3D Printing - John Whinnen Electronic Design through Collaboration - Mark Steiner CONFERENCE RECEPTION Thursday September 15 Flex PCB Design and Assembly with Dale Lee Root Cause Analysis for Reliability Issues in Electronics Packaging with Dr S Maniam Ramkumar Lunchtime Presentation - Internet of Things - Simon Blyth Lunchtime Presentation - Internet of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon SOL			9.30 am to 5.00 pm	610	9
High Performance Digital Control with Dr Hamish Laird Ramkumar High Performance Digital Control with Dr Hamish Laird Ramkumar IPC-A-610 Acceptability of Electronic Assemblies Day 2 of a 3 day course Lunchtime presentation Getting your product to market faster with 3D Printing - John Whinnen Electronic Design through Collaboration - Mark Steiner CONFERENCE RECEPTION Flex PCB Design and Assembly with Dale Lee Thursday September 15 Root Cause Analysis for Reliability Issues in Electronics Packaging with Dr S Maniam Ramkumar Lunchtime Presentation - Internet of Things - Simon Blyth Where'd the Heat Go? — Impacts of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon SOL			8.30 am to 4.30 pm	DFM	3
IPC-A-610 Acceptability of Electronic Assemblies Day 2 of a 3 day course Lunchtime presentation Getting your product to market faster with 3D Printing - John Whinnen Electronic Design through Collaboration - Mark Steiner CONFERENCE RECEPTION Flex PCB Design and Assembly with Dale Lee 8.30 am to 12 noon FLX Root Cause Analysis for Reliability Issues in Electronics Packaging with Dr S Maniam Ramkumar Lunchtime Presentation - Internet of Things - Simon Blyth Lunchtime Presentation - Internet of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon QFN			8.30 am to 4.30 pm	SMT	4
Day 2 of a 3 day course **Lunchtime presentation** Getting your product to market faster with 3D Printing - John Whinnen Electronic Design through Collaboration - Mark Steiner **CONFERENCE RECEPTION** 6.15 PM REC **CONFERENCE RECEPTION** 6.15 PM REC Thursday September 15 Flex PCB Design and Assembly with Dale Lee **Root Cause Analysis for Reliability Issues in Electronics Packaging with Dr S Maniam Ramkumar **Lunchtime Presentation - Internet of Things - Simon Blyth** 12.30 pm IOT Where'd the Heat Go? - Impacts of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon SOL		High Performance Digital Control with Dr Hamish Laird	8.30 am to 4.30 pm	DIG	5
Flex PCB Design and Assembly with Dale Lee Root Cause Analysis for Reliability Issues in Electronics Packaging with Dr S Maniam Ramkumar Lunchtime Presentation - Internet of Things - Simon Blyth Where'd the Heat Go? – Impacts of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield Pam to 12 noon SOL		•	8.30 am to 4.30 pm	610	
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Thursday September 15 Flex PCB Design and Assembly with Dale Lee Root Cause Analysis for Reliability Issues in Electronics Packaging with Dr S Maniam Ramkumar Lunchtime Presentation - Internet of Things - Simon Blyth Umbere'd the Heat Go? — Impacts of Thermal Connections in Today's Demanding Designs — Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon SOL		Electronic Design through Collaboration - Mark Steiner	5.00 pm	EDC	6
Root Cause Analysis for Reliability Issues in Electronics Packaging with Dr S Maniam Ramkumar Lunchtime Presentation - Internet of Things - Simon Blyth Where'd the Heat Go? - Impacts of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon RCA 1.15 to 4.30 pm WHG		CONFERENCE RECEPTION	6.15 PM	REC	
Packaging with Dr S Maniam Ramkumar Lunchtime Presentation - Internet of Things - Simon Blyth Where'd the Heat Go? - Impacts of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon RCA 1.15 to 4.30 pm QFN Soldering Best Practice and Equipment Tips for Higher Yield		Flex PCB Design and Assembly with Dale Lee	8.30 am to 12 noon	FLX	7
Where'd the Heat Go? – Impacts of Thermal Connections in Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon SOL			8.30 am to 12 noon	RCA	6
Today's Demanding Designs - Dale Lee Characterizing and Minimizing Voids in Quad Flat No-Lead Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon SOL		Lunchtime Presentation - Internet of Things - Simon Blyth	12.30 pm	IOT	7
Pack (QFN) Device Assembly Using Pb-Free Solder Alloys Soldering Best Practice and Equipment Tips for Higher Yield 9 am to 12 noon SOL		·	1.15 to 4.30 pm	WHG	8
g am to 12noon SOI			1.15 to 4.30 pm	QFN	6
and Reliability with IPC Trainer Mark Dobson		Soldering Best Practice and Equipment Tips for Higher Yield and Reliability with IPC Trainer Mark Dobson	9 am to 12noon	SOL	7
ESD Control Workshop including IPC Certification 1.00 to 4.00 pm ESD with IPC Trainer Mark Dobson		·	1.00 to 4.00 pm	ESD	8
IPC-A-610 Acceptability of Electronic Assemblies Day 3 of a 3 day course 8.30 am to 4.00 pm 610			8.30 am to 4.00 pm	610	
					10
VENUE INFORMATION		VENUE INFORMATION			11

CODE: DFM

Design for Excellence: DFM (Design for Manufacturing), DFR (Design for Reliability), DFA (Design for Assembly) and More

Dale Lee, Plexus Corporation

Wednesday September 14, 2016 8.30 am to 4.30 pm

Dale Lee is a Staff DFX Process Engineer with Plexus Corporation primarily involved with DFX analysis and definition/correlation of design, process, legislative and tooling impacts on assembly processes and manufacturing yields. Prior to Plexus Corporation Dale worked for Boston Scientific, Unisys, Iomega, Motorola, Texas Instruments, Evans and Sutherland, MSL/Celestica Dale is a past recipient of the Surface Mount Technology Association's "Excellence in Leadership" award and active with SMTA, INEMI, and IPC. Dale has served on the SMTA Board of Directors.

Dale has authored, instructed and spoken frequently on advanced SMT packaging, PCB and SMT design, assembly, DFM/DFX, and rework.



Part 1: Printed board and assembly designs today are increasing more complex not only due to increased functional requirements but with legislative requirements, component packaging technologies, laminate materials, copper thickness, fabrication methods, assembly processes, industry standards and their interactions. With the increase in complexity comes the increase potential for unplanned interactions that may impact PCB fabrication technologies, supply chain design, manufacturability, assembly producibility and/or reliability. This course will review elements and opportunities of conducting a design for excellence program including; defining how success is measured, supplier documentation accuracy, globalization issues, understanding of PCB fabrication technologies and process, and limitation of industry standards (fabrication, design, assembly).

What You Will Learn:

- Understanding of errors in component supplier documentation
- PCB laminate material types and impacts on function and reliability
- Copper thickness impacts on fabrication process
- PCB design complexity impacts on fabrication costs and reliability
- > Limitation of industry standards

Part 2: Today's design tolerances have impacted traditional assembly processes with very tight solder application, component placement and soldering constraints. Traditional design for excellence programs have focused on matching the design to manufacturing, assembly, test and reliability requirements. However, with the high diversity of component packages, decreased spacing between components, increased complexity of printed boards, increased diversity of materials and reliability requirements, it is not feasible to achieve a high-yielding manufacturing process. This course will introduce the concept of design-for-matched-process (DFMP) and provide examples of several opportunities within the DFMP for yield improvement through manufacturing tooling design, SMT and PTH assembly process matching, environmental controls and test fixture development.

What You Will Learn:

- SMT assembly design impacts
- > Through hole component (Wave/Selective) solder design impacts
- PCB design impacts to assembly: thermal balance, trace routing,
- Process tooling (assembly/test) impacts
- Impacts of design on process control issues; paste volume, SMT and PTH thermal shock, reflow warpage
- Design for cleaning issues
- Limitation of industry standards

Who Will Benefit:

Designers, Manufacturing/Process, Quality and Reliability Engineers, Managers or Technicians that are involved with the design, fabrication, assembly or test of printed board assemblies.

SMT and Through Hole Defect Analysis and Process Troubleshooting

Dr S. Manian Ramkumar, Rochester Institute of Technology Wednesday, September 14 8:30am - 4.30pm

Dr. Ramkumar is a Professor at the Rochester Institute of Technology (RIT) and is Director of the Center for Electronics Manufacturing & Assembly (CEMA). He teaches courses in surface mount electronics packaging and manufacturing automation. He was instrumental in developing CEMA at RIT. CEMA is equipped with assembly and failure analysis equipment, to support hands-on training and applied research projects for industry. Dr. Ramkumar has been the principal investigator for several applied research projects. He has presented technical papers at the SMTA, APEX, IMAPS, ASME and IEEE conferences. He also teaches Surface Mount Technology (SMT) and Advanced Packaging courses at the IPC-APEX and SMTA shows and for various companies on-site. He has taught in India many SMT workshops in the past and has been a frequent presenter at the SMTA-India Chapter events and also provided key note addresses. Dr Ramkumar is a Master of Engineering in Manufacturing Engineering, Rochester Institute of Technology and a PhD in Science Systems, State University of New York.



Course Objectives

Part 1 is aimed at providing a thorough understanding of the SMT and Through Hole defects and the various factors that influence the formation of the defects. Participants will be provided with an in-depth look at the possible root causes for defects and their influence on yield. The knowledge gained from this course will help companies enhance product development, and manufacturing yield. Part 2 of the workshop series will use case studies to teach participants a systematic approach to solve process problems and identify the true root cause(s) for defects.

Topics Covered

- **SMT and THT Process**
 - Assembly types and processes
- Factors influencing the process defects
 - o PCB related
 - Component related
 - o Materials related
 - o Equipment related
 - Possible root causes for defects based upon factors
- Process defects and definitions
 - o Identifying different defects
 - Process related
 - Supplier related
 - Employee/Knowledge related
 - **Environment related**

Part 2 is aimed at providing a good understanding of a systematic problem solving approach that can be used for troubleshooting the Surface Mount Technology (SMT) and Through Hole electronics packaging process, to avoid defects. This hands-on problem solving session will engage the participants actively using case studies. The participants will work in teams and solve the problem by thoroughly defining the problem, finding the true root causes and determining the appropriate fix. The knowledge gained from this workshop will help companies enhance product development and manufacturing yield through systematically addressing the root causes of any problem.

Topics Covered

- Creating a problem statement
 - o Initial problem definition
 - Ideal vs. actual
 - Data collection
 - Questioning to the void (data collection)
- Organizing the data related to the problem
 - "Is" and "Is Not" comparison
 - Differences influencing the "Is" and "Is Not"
 - o Changes influencing the differences
- Identifying probable root cause(s)
 - o Testing the possible root causes
 - Selecting the most probable cause
 - Verifying the most probable cause

- Process flow mapping
- o What? Where? When? Extent?
- Final problem definition (object and defect)
- Finding a fix for the root cause
 - Developing and classifying the objectives (Must and Want)
 - Identifying and evaluating the alternatives
 - o Identify the risks with alternatives Final decision for a fix
 - Testing the fix

CODE: DIG

High Performance Digital Control

Dr Hamish Laird, ELMG Digital Power Wednesday September 14 8.30 am to 4.00 pm

This presentation is aimed at intermediate level power engineers and addresses techniques used to successfully implement digital control for power electronic converters. The presentation will examine the key components of the controller - digital (PWM and VPO) modulators, compensator pole zero placement, compensator numeric precision issues, single sample noise and anti-aliasing filter design.

Digital pulse width modulators (PWM) and digital variable period oscillators (VPO) have different non-linear frequency response characteristics from equivalent analogue systems. The effect of these differences on the control is discussed and spectral-shaping design methods to improve performance of the digital modulators will also be discussed.

We will then look at the design of the compensator by directly placing the digital poles and zeros. By translating the pole and zero positions directly into digital filter coefficients for the digital compensator, the translation of analogue coefficients to digital is avoided.

A method that requires no coding or simulation for determining numeric precision issues in the digital compensator coefficients will then be presented. As most systems require integrators we will discuss the most suitable forms of digital integrators. The precision issues specific to digital integrators and methods to reduce these will be examined in detail.

Finally managing single sample errors, which have no analogue equivalent and the choice of anti-aliasing filters will be described.

Dr Hamish, ELMG Digital Power NZ is involved in developing digitally controlled power converters and controllers for converters. He founded ELMG Digital Power in 2001 to provide high value services and training to companies developing digital power electronics. ELMG has completed power electronic product development for reactive power control, motor drives, motor starters and medium voltage motor starters and medical devices. In 1998 Hamish commenced study for his PhD degree. The title of the thesis completed in 2001 was "Modelling and measurement of non-linear rectifier loads and their interaction with shunt active filters". Hamish is the author of 16 academic papers on digital power electronics and power quality.

In 1996 Hamish joined Eurotherm Drives (now Parker Hannifin SSD Drives), Littlehampton, England where he worked in product development of large scale manufactured digital and analogue DC and digital AC motor drives. After traveling in the USA Hamish worked at GEC Alsthom (now Alstom) Transmission and Distribution Power Electronics Systems, Stafford, England, UK in 1995 and 1996. Here Hamish worked on large scale HVDC transmission power converter systems and SVC reactive power control systems. From 1992 to 1994 he worked as a design engineer developing induction motor starters and variable speed drives at AuCom Electronics, Christchurch, New Zealand.

Hamish Laird studied for the Bachelor of Electrical and Electronic Engineering at the University of Canterbury, Christchurch, New Zealand from 1987 to 1990. Immediately following this he completed his Master's at the same University.

Getting your product to market faster with 3D Printing

Wednesday September 14 12.45 to 1.30 pm

John Whinnen, Objective3D Printing Solutions

CODE: 3DP

This presentation looks at the use of 3D printing technologies for the Electronics Industry. Learn how 3d printing is used for fit, form and function testing, creating prototypes using same material as the finished product, experiment with different materials including clear, flexible and rigid. Find out more about and in-house solutions versus outsourcing and lot's more.

Who should attend:

- Electrical & Mechanical Engineers
- Manufacturing Engineers
- Test Engineers
- Design Engineers
- Engineering Management
- R&D Professionals
- Anyone else who needs an introduction to 3D printing

CODE: EDC

CODE: RCA

CODE: QFN

Electronic Design through Collaboration

How to achieve better and faster designs

- Mark Steiner Wednesday September 14 at 5.00 pm

The pool of companies and engineers in Australia is shrinking by the year. Finding good engineers and companies who can design and build new products are limited. So what can we do about it? How can we still be innovative and manufacture here in Australia? This presentation will give you some ideas, solutions and tips what we all can do about it together.

Root Cause Analysis for Reliability Issues in Electronics Packaging

Dr S Manian Ramkumar, Rochester Institute of Technology

September 15, 2016 Half Day 8.30 am to 12.00 pm

Dr. Ramkumar will discuss the following topics:

Quality v. Reliability, Failure Modes and Mechanisms, Failures and Root Causes, and Reliability Testing.

In this presentation failure, reliability, and quality are defined as:

- Failure being the inability for a product to perform its function—a reliable product will have a failure rate close to zero, providing good quality over time.
- Quality is a measure of the conformance to product specifications at any given instant in time (does the product do what it was intended to do?).
- Reliability is a measure of the product's ability to perform the desired function, without failure, understated conditions, for a stated period of time.

Quality and reliability despite having differing definitions are synonymous with one another i.e. you cannot have reliability without quality and vice versa.

A quality product will fetch you customers, but high reliability of the product will keep customers coming back to buy more product. This will be one of the main themes echoed throughout the presentation. Simply put, reliability is considered to be quality over a period of time.

Quality is at time "zero" (when the product is being made) and reliability is when you have created a quality product, sent it to the customer, and it is operating properly in the field. It's at this point you are looking for the ability of the product to function, without failure, for a given period of time.

Most of the quality concerns, and the root cause for quality and therefore reliability issues, will occur at the manufacturing stage. It is at this point that any issues found are corrected and in-circuit and functional testing should be done. It is crucial for both your budget and time-to-market that testing is done accurately and as quickly as possible. It is after this stage we will focus on the concept of reliability.

At every stage of the product development cycle, producing a quality product should be the goal, with a continuous improve plan in order to achieve higher levels of reliability. With electronics, this is even more significant. Consider this, electronics are made of multiple components, and all of these components have their own standards of reliability which then define the reliability of the electronic product/system. The products you use to create any of these components or product pieces are integral to achieving your quality and/or reliability standards.

Characterizing and Minimizing Voids in Quad Flat No Lead Pack (QFN) Device Assembly Using Pb Free Solder Alloys

Dr S Manian Ramkumar, Rochester Institute of Technology Thursday September 15, 2016 Half Day 1.00 to 4.30 pm

Quad Flatpack No lead (QFN) packages have become a popular choice in electronics packaging due to their small form factor. They are also gaining rapid industry acceptance because of its excellent thermal and electrical performance. The bottom side of the QFN package has a large thermal pad. This exposed die attach pad effectively conducts heat to the PCB and also provides a stable ground connection. Effective soldering of this surface to the pad on the PCB is required for good thermal dissipation and component functionality. The exposed thermal pad presents various challenges during the surface mount assembly process. One major challenge is solder void formation. Voids are primarily formed due to the entrapment of volatiles in flux outgassing during the reflow process. The primary objective of this study is to determine optimal parameters to minimize void formation in QFN packages (QFN16, QFN20, QFN28 and QFN32), specifically the reflow profile, lead-free solder paste and stencil aperture opening for the thermal pad. A systematic DOE based approach was used to arrive at conclusions, using the ratio of void volume on the thermal pad to the actual volume of solder paste printed as the response variable. Various graphs are presented to understand the impact of different parameters. Interaction graphs are used to determine optimal settings for each parameter.

CODE: FLX

CODE: SOL

CODF: IOT

Flex PCB Design and Assembly - Dale Lee

Thursday September 15 Half Day 9 am to 12 noon

The increase of wearable medical and consumer devices, increased automotive and IOT devices has increased the demand and range of use for flexible and rigid-flex PCB and assembly designs beyond the traditional aerospace, defense, implantable medical and small consumer electronic devices. With flex/rigid-flex PCB designs, additional design, fabrication and assembly guidelines are required versus traditional rigid board designs to meet product performance requirements.

This presentation and discussion will provide an introduction and images to flexible circuit design guidelines, fabrication requirements/limitations/construction process, rigid vs flex PCB differences, assembly and reliability issues and impacts and highlight differences with traditional rigid board design/assembly. You will gain an understanding of design, reliability, and fabrication, assembly techniques for flex and rigid-flex PCB and assemblies.

Areas Covered in the Session:

- •IPC Defined Types of Flex Designs
- •Unique Requirements with Flex Designs
 - Bend Area Conductors
 - Connector Termination
 - Stiffeners
 - Bend Impacts
- Types of Flex Materials
- Bend Radius Limitations
- Assembly Process
 - Assembly Tooling
 - Assembly Tolerances Stencil/Component Placement
 - Depanelization Process

Who Will Benefit:

- •Design Engineers •Flex Designers •Quality Engineers/Technicians •Manufacturing/Process Engineers/Technicians
- •Reliability Engineers •Anyone wanting to learn how to understand flexible PCB's and assembly

Soldering Best Practice and Equipment Tips for Higher Yield and Reliability

Mark Dobson, Certified IPC Trainer

Thursday September 15 9 am to 12 noon

This half day presentation will focus on recommendations for best practice soldering (hand and automated) to optimise yield and reliability. It will include tips on selecting equipment and what you need to look out for depending on your end product. Mark will also address the requirements of the 7711/21 you need to be aware of in particular in relation to optimum temperatures and acceptability. In addition to providing information to improve soldering performance this presentation will also assist in equipping you with knowledge to go to the Electronex exhibition floor and assess equipment and its suitability for your workplace.

Internet of Things

Simon Blythe LX Group

Thursday September 15 at 12.30 pm

The Internet of Things (IoT) is the network of physical devices, vehicles, buildings and other items—embedded with electronics, software, sensors, actuators, and network connectivity that enable these objects to collect and exchange data. The IoT allows objects to be sensed and controlled remotely across existing network infrastructure, creating opportunities for more direct integration of the physical world into computer-based systems, and resulting in improved efficiency, accuracy and economic benefit; when IoT is augmented with sensors and actuators, the technology becomes an instance of the more general class of cyber-physical systems, which also encompasses technologies such as smart grids, smart homes, intelligent transportation and smart cities. Each thing is uniquely identifiable through its embedded computing system but is able to interoperate within the existing Internet infrastructure. Estimates are that the IoT will consist of almost 50 billion objects by 2020

CODE: ESD

Electrostatic Discharge Control (ESD)

Mark Dobson, IPC Trainer Thursday September 15 1.00 to 4.00 pm

This half day workshop explains the necessary information operators need to understand in order to control charge build-ups and prevent costly damage to electronic components and assemblies.

The training covers:

- the physics of static electricity
- how static charges damage components
- grounding, wrist straps, shoe grounding, safe clothing and conductive smocks
- testing
- ESD safe work areas
- elimination of static generating materials
- controlling charge build-ups
- activities that create static electricity
- proper handling/storage and transportation of ESD sensitive devices

The IPC program utilised in this course was produced in co-operation with the ESD Association and satisfies the ANSI/ESD S20.20 Initial ESD Awareness and Prevention Training requirement. A comprehensive training video is used in this training.

IPC Certification: The Certification Test includes questions designed to measure operator proficiency in ESD prevention. A Certificate will be issued to students scoring above 70%. The course is led by Mark Dobson, an experienced ESD Control instructor who is also a Certified IPC Trainer (CIT).

In addition to the training Mark will highlight essential accessories and equipment which will provide ESD protection in the workplace.

Where'd the Heat Go? - Impacts of Thermal Connections in Today's Demanding Designs

CODE: WHG

Dale Lee Thursday September 15 Half Day 1.15 pm to 4.30 pm

The demands for increased design densities for electronic assemblies have impacted the effects of functional performance thermal management demands and ability to form reliable surface mount and through-hole component solder connections. Today, many components have incorporated thermal management solutions into their designs (QFN, Thermal Pad SOIC, D-Pack, etc.)

This presentation will review embedded thermal management options utilized in design, impacts of thermal connections on through-hole and surface soldering processes, methods for identification of potential solder workmanship/reliability issues and some recommended potential design/assembly process solutions.

Areas Covered in the Session:

- •Typical Embedded Thermal Management Methods
 - Thermal Via's (Via in Pad –VIP)
 - Heat Slug / Copper Coin (Press Fit, Embedded, Surface Attached)
 - Thick Copper Layers/Plating
 - Metal Core Boards
- •Through-hole Soldering
 - Issues With Excessive Thermal Connection
 - Calculation of Soldering Process Thermal Load
 - Alternative Design/Process Methods
- SMT Soldering
 - Issues with Excessive Thermal Connection
 - Surface Imbalance
 - o Blind/micro-via in pad
 - Through-hole Via in Pad (Filled and Overplated)
 - o Through-hole Via in Pad (Unfilled)
 - o Stacked Via (Micro-Via on Buried Via)
 - Alternative Design/Process Methods

Who Will Benefit: • Manufacturing/Process Engineers/Technicians • Design Engineers

• Quality Engineers/Technicians • Reliability Engineers • Anyone wanting to learn about embedded thermal management methods and the impact on assembly processes

IPC A 610 Acceptability Of Electronic Assemblies Training and Certification

Tuesday September 13 to Thursday September 15 CODE: 610
Mike Ross, Master IPC Trainer

Please note: this is a three day program commencing on Tuesday September 13.

This is your opportunity to attain portable and internationally recognized certification as a Certified IPC Specialist (CIS) or Certified IPC Trainer (CIT) for the A-610 Acceptability of Electronic Assemblies – the most widely used standard published by the IPC with an international reputation as the source for end product acceptance criteria for consumer and high reliability electronic assemblies. This course is to the latest Revision F of the A-610 standard.

Certification will demonstrate your commitment to customer requirements and greatly assist any company dedicated to quality assurance initiatives. The IPC training and certification has immediate recognition, legitimacy and value with thousands worldwide having been trained and certified. The 610 course is modularised, topics include:

- Purpose and application of the IPC-A-610 standard
- > Hardware installation
- Soldering criteria including lead free connections
- Soldered requirements for connecting to terminals
- Soldered connection requirements for plated-through holes
- > Surface mounting criteria for chip components, leadless and leaded chip carriers
- Swaged hardware and heat sink requirements of mechanical assemblies
- Component mounting criteria for DIPs, Socket pins and card edge connectors
- Jumper wire assembly requirements
- Solder fillet dimensional criteria for all major SMT component groups
- > Soldering problems such as tombstoning, dewetting, voiding
- > Criteria for component damage, laminate conditions, cleaning and coating

Modules are:

M1: Policies & Procedures
M2: Purpose & Application of the 610
M3: Hardware Installation
M4: Soldering
M5: Terminal Connections
M6: Through-Hole Technology
M7: Surface Mount Assemblies
M8 Component Damage, PCBs & Assemblies
M9: Solderless Wire Wrap

CERTIFIED IPC TRAINER (CIT) CANDIDATES attaining the required pass marks will receive a kit of materials to conduct 610 CIS level training to the current Revision F Course.

RECERTIFICATION CANDIDATES - PLEASE CONTACT SMCBA OFFICE ON 03 9571 2200 OR EMAIL pollocka@smcba.asn.au FOR RECERTIFICATION DETAILS INCLUDING FEES

ELECTRONICS DESIGN & MANUFACTURE

CONFERENCE

CONFERENCE REGISTRATION

EARLY BIRD DISCOUNT DEADLINE - Register by 19 AUGUST 2016

Registration is available online at: https://register.smcba.asn.au/ or complete this form and return to SMCBA by:

Fax: 03 9571 3300 (Australia), +61 3 9571 3300 (International) Email: pollocka@smcba.asn.au

Post: PO Box 3140, MURRUMBEENA VIC 3163, Australia

NAME:	POSITION:									
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If you have any questions please contact SMCBA on 03 9571 2200 (Australia) or +61 3 9571 2200 (International).										
TICK BOX CONFERENCE SESSIONS		МЕМВЕ	R RATES	NON MEN	IBER RATES					
Rates are EXCLUSIVE of GST		Early Bird	After 19-Aug	Early Bird	After 19-Aug					
TUESDAY 13 SEPTEMBER 2016										
610S CIS Level – IPC-A-610 (3 day program)		\$850	\$900	\$1,000	\$1,100					
610T CIT Level – IPC-A-610 (3 day program)		\$2,500	\$2,600	\$2,750	\$2,850					
WEDNESDAY 14 SEPTEMBER 2016										
DFM Design for DFM, DFR, DFA and more		\$300	\$350	\$500	\$550					
SMT & Through Hole Defect Analysis + Process	s Troubleshooting	\$300	\$350	\$500	\$550					
DIG High Performance Digital Control		\$200	\$250	\$400	\$450					
3DP 3D Printing – Getting your product to market	faster	-	-	-	-					
EDC Electronic Design and Collaboration		-	-	-	-					
REC Electronex Reception ⁽¹⁾ at 6.15 pm	Described by	-	-	-	-					
(1) There is no cost for delegates to attend the Electro THURSDAY 15 SEPTEMBER 2016	тех кесериоп вистеді	stration is requ	irea.							
RCA Root Cause Analysis for Reliability Issues in Ele	ectronics Pkg(2)	\$175(2)	\$200(2)	\$275(2)	\$300(2)					
FLX Flex PCB Design and Assembly (2)	cettories ring.	\$175(2)	\$200(2)	\$275(2)	\$300(2)					
SOL Soldering Best Practice and Equipment Tips (3))	\$125(2)	\$150(2)	\$225(2)	\$250(2)					
IOT Internet of Things		-	-	_	-					
QFN Quad Flat No-Lead Pack (QFN) Device Assemb	nly	\$125	\$150	\$225	\$250					
	, i y									
		\$125	\$150	\$225	\$250					
ESD Control Workshop and Certification		\$100	\$120	\$150	\$170					
⁽²⁾ Includes lunch in fee										
GET EARLY BIRD DISCOUNT & SAVE!!	Fee Payable (A\$)									
Register By 19th August	Plus 10% GST (A\$)									
View SMCBA Membership information at www.smcba.asn.au/mform.pdf	TOTAL (A\$)									
All delegates are provided with tea / coffee breaks and lunch is included for all sessions starting in the morning. ELECTRONEX REGISTRATION: All delegates are automatically registered to attend the Electronex Exhibition – separate registration is NOT required. PAYMENT: On receipt of your registration you will be sent a confirmation together with a Tax Invoice requiring payment within 7 days. Payment methods will be detailed on invoice. CANCELLATION POLICY: Cancellation on or after 6 September-2016 will incur \$110 cancellation fee (includes proceedings). TRANSFER: You can transfer your registration to another party without any penalties. CONFIRMATION: Confirmation of registration requires acceptance of the above cancellation policy. Please sign and date below to complete your Conference Registration. Date:										
(Person Registering)										

CONFERENCE VENUE AUSTRALIAN TECHNOLOGY PARK (ATP) EVELEIGH, SYDNEY

The SMCBA Electronics Design and Manufacture Conference and Electronex Expo will be held in the ATP conference and exhibition centre - entry via Bay 8.

A map can be downloaded from http://www.smcba.asn.au/ATPmap.pdf

How to get there: By car/taxi: Only a few minutes drive from Sydney CBD and about 15 minutes from the airport.

Travel along Botany Road and turn at Henderson Road. By train: 8 minutes walk from Redfern Station

Parking: Undercover and outdoor parking is available at the venue, take a ticket at the boom gate and pay stations are available in the Electronex entrance fover

Accommodation: The are a couple of nearby hotels and it is also convenient to stay at an inner city hotel and commute to the ATP by train or taxi. Some hotels are listed at http://www.smcba.asn.au/accommodationATP.pdf **Conference Registration:** Please complete the form on the last page of this program and return to the SMCBA.



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